LOGIC SYNTHESIS AND VERIFICATION ALGORITHMS

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Springer, 2006. Soft cover. Book Condition: New. In the last decade logic synthesis has gained widepsread acceptance by designers. Formal verification is now advancing along the same path. Computer aided design tools for logic synthesis and verification have become the primary instrument for coping with the ever increasing complexity of designs, and ever more stringent time-to-market constraints. Effective design must be based on thorough understanding of the capabilities, limitations, and algorithmic principles employed by these tools. In this book we provide a foundation for such understanding. Logic Synthesis and Verification Algorithms blends mathematical foundations and algorithmic developments with circuit design issues. Each new technique is presented in the context of its application to design. Through the study of optimal two-level and multilevel combinational circuit design, the reader is introduced to basic concepts, such as Boolean algebras, local search, and algebraic factorization. Similarly, through the study of optimal sequential circuit design, the reader is introduced to graph algorithms, finite state systems, and language theory. Throughout the book, recurrent themes such as branch and bound, dynamic programming, and symbolic implicit enumeration are used to establish optimal design principles. Circuit designers and CAD tool developers alike will find Logic Synthesis and Verification Algorithms useful as an introductory and reference text. The rich collection of examples and solved problems make this book ideal for self study. Because of its careful balance of theory and application, Logic Synthesis and Verification Algorithms will serve well as a textbook for upper division and first year graduate students in electrical and computer engineering.

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